**In the Specification**

Please amend paragraphs [0008]-[0009] as indicated below:

[0008] While the prior art arrangement shown in FIG. 2 performs acceptably within a memory array, ~~two~~Two problems of the prior art arrangement of FIG. 2 make it unsuitable for use in high-speed SerDes cores operating at signal switching speeds above about 500 MHz. First, the MOSFETs used as transmission gates of the default signal path, for example gates T21 of multiplexer 20, introduce jitter noise which restrains the bandwidth of the signals passed from input signal lines di1-di4 to do1-do4. Second, the redundancy signal path from redundancy signal line rdi to output signal line suffers from high parasitic junction capacitance. The redundancy signal line rdi is connected to all redundancy transmission gates, i.e. gates T12, T22, T32 and T42, such that all of the MOSFETs of the transmission gates contribute to the parasitic junction capacitance. Such parasitic junction capacitance reduces the transmission bandwidth of signals on the redundancy signal input line rdi even more so than the jitter noise caused by the transmission gates of the default signal path. Both of these problems make redundancy replacement arrangements using MOSFET transmission gates unsuitable for signal switching speeds above about 500 MHz.

[0009] Therefore, it would be desirable to provide a redundancy replacement arrangement for a high-speed communications circuitry adapter. It ~~it~~ would further be

desirable to provide a redundancy replacement arrangement suitable for high speed communications circuitry operating above about 500 MHz.